IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	: Payman Zarkesh-Ha, et al.
Appl. No.	: 10/764,803
Filed	: January 26, 2004
Art Unit	: 2823
Examiner	: Kim, Su C
Title	: FIELD PROGRAMMABLE PLATFORM ARRAY
Attorney Docket No.	: 02-5938
Confirmation No.	: 9749

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO THE FINAL OFFICE ACTION DATED NOVEMBER 18, 2009

CERTIFICATE OF MAILING/TRANSMISSION (37 C.F.R. § 1.8)

I hereby certify that on the date specified below, this correspondence is being filed with the United States Patent and Trademark Office Electronic Filing System.

/shirley dunne/ Date: February 9, 2010
Shirley Dunne

Dear Examiner:

This is in response to the Final Office Action dated November 18, 2009, for which the three-month shortened statutory period for reply is set to expire on February 18, 2010. While Applicants believe that no extension of time for response is necessary, should the Office determine that any additional fees are necessary for this response, the Commissioner is hereby authorized to charge any deficiencies to Deposit Account No. 19-4882.

A **Listing of Claims** begins on page 3 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Entry of the Amendments below and consideration of the Remarks that follow is respectfully requested.

AMENDMENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method for providing field programmable platform array units, comprising:

cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer, N and M being positive integers, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units, said plurality of platform array units having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor, and interconnect between said plurality of platform array units being pre-routed on chip; and

packaging and testing said N by M array of platform array units;

wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal;

wherein said single platform array unit platform is a digital signal processing (DSP) platform;

wherein said interconnect between said plurality of platform array units is at least one of direct, via bus-bars, and via network on chip.

2. (Original) The method of claim 1, further comprising:

programming said N by M array of platform array units by said customer.

3. (Original) The method of claim 2, wherein said programming is performed for at least one of unit specialization, unit role assignment, and inter-unit communications.

4. (Original) The method of claim 2, wherein said programming is performed with firmware.

5. (Canceled)

6. (Previously Presented) The method of claim 1, wherein said single platform array unit platform is a storage area network (SAN) platform.

7. (Canceled)

8. (Original) The method of claim 1, further comprising storing said field programmable platform array wafer.

9. (Previously Presented) A system for providing field programmable platform array units, comprising:

means for cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer, N and M being positive integers, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units, said plurality of platform array units having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor, and interconnect between said plurality of platform array units being pre-routed on chip; and

means for packaging and testing said N by M array of platform array units;

wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal;

wherein said single platform array unit platform is a digital signal processing (DSP) platform;

wherein said interconnect between said plurality of platform array units is at least two of direct, via bus-bars, and via network on chip.

10. (Original) The system of claim 9, further comprising:

means for programming said N by M array of platform array units by said customer.

11. (Original) The system of claim 10, wherein said programming is performed for at least one of unit specialization, unit role assignment, and inter-unit communications.

12. (Original) The system of claim 10, wherein said programming is performed with firmware.

13. (Canceled)

14. (Previously Presented) The system of claim 9, wherein said single platform array unit platform is a storage area network (SAN) platform.

15. (Canceled)

16. (Original) The system of claim 9, further comprising means for storing said field programmable platform array wafer.

17. (Previously Presented) A semiconductor device, comprising:

a plurality of platform array units within a single platform array unit platform having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor;

wherein interconnect between said plurality of platform array units being pre-routed;

wherein said single platform array unit platform is a digital signal processing (DSP) platform;

wherein encapsulation of lower copper metal layers of said semiconductor device is preserved by a standard die seal;

wherein said interconnect between said plurality of platform array units is at least one of via bus-bars and via network on chip.

18. (Previously Presented) The semiconductor device of claim 17, wherein said semiconductor device includes top aluminum pads and said top aluminum pads of said semiconductor device are used as a routing layer for the pre-routed interconnect between said plurality of platform array units.

19. (Canceled)

20. (Previously Presented) The semiconductor device of claim 17, wherein metal bumps of said semiconductor device are used as a routing layer for the pre-routed interconnect between said plurality of platform array units.

21. (Previously Presented) The semiconductor device of claim 17, wherein a copper layer within said semiconductor device is used as a routing layer for the pre-routed interconnect between said plurality of platform array units.

22. (Previously Presented) The semiconductor device of claim 17, wherein a polysilicon layer of said semiconductor device is used as a routing layer for the pre-routed interconnect between said plurality of platform array units.

23. (Previously Presented) The semiconductor device of claim 17, wherein a silicon layer of said semiconductor device is used as a routing layer for the pre-routed interconnect between said plurality of platform array units.

24. (Original) The semiconductor device of claim 17, wherein said plurality of platform array units are configured by external software programming.

REMARKS/ARGUMENTS

Claims 1, 2-4, 6, 8-12, 14, 16-18 and 20-24 are now pending in this application. Claims 1, 9 and 17 are independent claims. Claims 5, 7, 13, 15 and 19 have been cancelled.

Claim Rejections - 35 USC § 103(a)

Claims 1-4, 8-12, 16, 17 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Voogel, US 6,362,651 (hereinafter: Voogel) in view of Hongo et al., US 2003/0143971 (hereinafter: Hongo) and further in view of Glenn et al., US 6,962,829 (hereinafter: Glenn). (Pending Office Action, Page 2). Claims 6 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Voogel, in view of Hongo, in view of Glenn, in further view of Mastro et al., US 2002/0091977 (hereinafter: Mastro). (Pending Office Action, Page 5). Claims 18 and 20-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Voogel, in view of Hongo, in view of Glenn, in view of Lee et al, US 6,222,212 (hereinafter: Lee). (Pending Office Action, Page 5). Applicants respectfully traverse these rejections.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicants respectfully submit that the claims rejected under this section include elements that have not been disclosed, taught or suggested by any of the references cited by the Patent Office, either alone or in combination.

Independent Claims 1, 9 and 17 each generally recite:

> "interconnect between said plurality of platform array units being pre-routed on chip."

In the present invention, the interconnect between the plurality of platform array units may be pre-routed on chip for avoiding paying for off-chip overhead (e.g. package misalignment, ESD protection, or the like). (Present Application, Paragraph 0016). The Patent Office cites Voogel as teaching the

above-referenced elements of the present invention. (Pending Office Action, Page 3). However, the Patent Office-cited portion of Voogel merely discusses a conductor which extends across scribe line space. (Voogel, Column 8, Lines 39-40). Voogel does not disclose, teach, or suggest an interconnect being pre-routed on chip as in the present invention. Nowhere in any of the cited references, either alone or in combination, are the above-referenced elements of the present invention either disclosed, taught, or suggested.

Based on the above rationale, the Patent Office has failed to make a *prima facie* case of obviousness against claims 1, 9 and 17. Thus, claims 1, 9 and 17 should be allowed over the prior art of record. Further, Claims 2-4, 6 and 8 (which depend from Claim 1), Claims 10-12, 14 and 16 (which depend from Claim 9) and Claims 18 and 20-24 (which depend from Claim 17) should also be allowed.

CONCLUSION

In light of the forgoing, reconsideration and allowance of the pending claims is earnestly solicited.

Respectfully submitted on behalf of
LSI Logic,

By: /jeffrey m andersen/
Jeffrey M. Andersen
Reg. No. 52,558

Dated: February 9, 2010

Jeffrey M. Andersen
SUITER • SWANTZ PC LLO
14301 FNB Parkway, Suite 220
Omaha, NE 68154
(402) 496-0300 telephone
(402) 496-0333 facsimile